UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,065	03/30/2006	Theodore J. Letavic	PHUS030375	9391

65913 7590 02/27/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
02/27/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/574,065	LETAVIC, THEODORE J.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/30/3006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because:

In Fig. 1, the drain region is missing and the drain electrode is referred to with a wrong numeral.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1-10 are objected to because of the following informalities: claim 1 recites multiple terms of "a first (or second) conductivity type", but fails to clarify the relationship between or among these first (or second) conductivity types.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the subject matter that "a field plate connected either to said source region or said gate electrode", which may implicate that the field plate as a whole is connected to the recited source region or gate electrode; but it appears to contradict to the subject matter also recited in the claim that "said field plate comprises a first layer of plural metallic regions which are isolated laterally from one another by spaces". It is not clear whether each of the metallic regions is connected to the recited source region or gate electrode, given that each of these metallic regions is a part of the recited field plate that has such connection as implicated with the recited term of "connected".

Claim Rejections - 35 USC § 102 and/or § 103

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 9, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Akiyama (US 2002/0043699).

Akiyama discloses a lateral thin-film Silicon-On-Insulator (SOI) device (Figs. 2-5, 10 and 12), comprising: a semiconductor substrate (100), a buried insulating layer (101) on said substrate, and a lateral MOS transistor device in an SOI layer on said buried insulating layer and having a source region of a first type conductivity (52; p type) formed in a body region of a second type conductivity (4; n type), a lateral drift region of a second type conductivity (n type; a portion of 102 that is between regions 4 and 7; and/or, a portion of 102 that is directly under the "P-" region 7; they each can naturally function as the lateral drift region as it is in contact with the body region and the two have a same conductivity type) adjacent said body region, a drain region ("P+" region in 7 or 32) of a first conductivity and laterally spaced apart from said body region by said

lateral drift region, a gate electrode (a portion of 10 that has direct contact with the underlying gate dielectric GX) insulated from said body region and drift region by an insulation region (GX), and a field plate (a portion of 10 that is above the field oxide layer FLX, plus MEP2) connected to said gate electrode and extending substantially over said lateral drift region, wherein said field plate comprises a first layer of plural conductive regions which are isolated laterally from one another by spaces, which naturally form a substantially linear lateral electric field distribution.

The gate electrode layer (10) and the first layer of field plate (MFP2) is formed with a polysilicon conductive layer in Akiyama; and such a polysilicon conductive layer is commonly regarded as a metallic layer in the art, as it is always heavily doped and have a conductivity property that is substantially metallic. And/or, the device formed in Akiyama is a MOS device, wherein the letter "M" (in the term of "MOS") stands for metal for the gate layer, which is commonly formed of a heavily doped polysilicon layer.

Or, in the alternative, although Akiyama does not expressly disclose that the conductive regions of the field plate (MFP2) and/or gate electrode (10) can be formed of a metallic material (a material from the metal elements), it is noted that it is well known in the art that a field plate and/or a gate electrode can be desirably formed of a metallic material so as to achieve increased conductivity therein.

Therefor, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Akiyama with the conductive regions of the field plate (MFP2) and/or gate electrode (10) therein being formed with a metallic

material, so that a device with desired high conductivity in the field plate and/or gate electrode would be obtained, as it has been held that:

The selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

Regarding claims 2 and 3, it is further noted that the isolated conductive regions (MFP2) in Akiyama are isolated from one another by a dielectric layer (IZ), and the field plate in Akiyama can further comprise another layer of plural metallic regions (MFP1) located above said spaces, laterally isolated from one another, and isolated from the conductive regions of said first layer by said dielectric layer.

7. Claims 4-8 and 10, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama in view of William (William et al., US 5,374,843) and/or Letavic (Letavic et al., US 6,127,703), or, in the alternative, as being unpatentable over Letavic in view of Akiyama and/or William.

The disclosure of Akiyama is discussed as applied to claims 1-3 and 9 above.

Although Akiyama does not expressly disclose that the dielectric layer can be formed of a silicon-rich nitride layer and/or that the drift region can have linearly-graded charge profile, one of ordinary skill in the art would readily recognize that such silicon-rich nitride layer can be desirably formed so as to increase the breakdown voltage, as readily evidenced in William (see col. 11, line 67, through col. 12, line 29); and that such linearly-graded charge profile can be desirably formed so as to achieve better performance, as evidenced in Letavic (see the drift region 32 in Figs. 1 and 2, which

have the same MOSFET device structure as that in the instant invention, except the recited field plate).

Therefor, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Akiyama with the dielectric layer being formed of a silicon-rich nitride layer and/or with the drift region having a linearly-graded charge profile, per the teachings of William and/or Letavic, so that a MOSFET device with increased breakdown voltage and/or improved performance would be obtained.

Or, in the alternative, it would also have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the field plate structure of Akiyama and/or the silicon-rich nitride layer of William into the device of Letavic, so that a MOSFET with improved and/or further improved breakdown voltage would be obtained.

Regarding claim 5, it is noted that at least in Akiyama there further has another dielectric layer (FLX) provided between said field plate and said MOS transistor device.

Regarding claim 7, it is noted the substantially linear lateral electric field distribution in the above collectively taught device would naturally follow an electric field in said drift region, in a manner substantially same as that in the instant invention.

Regarding claim 10, it is further noted that it is art known that a MOSFET design workable with a first polarity can be readily converted to another workable MOSFET with the opposite polarity by simply switching each of the doped regions to the opposite conductivity type, so as to obtain a MOSFET with the desired polarity.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
Primary Examiner, Art Unit 2811
February 16, 2008